Chettinad College of Engineering & Technology

Department of Electronics and Communication Engineering

EC8691-Microprocessors and Microcontrollers

UNIT I THE 8086 MICROPROCESSOR

MCQ BANK

1. A Microprocessor is a ---------- chip integrating all functions of a CPU of a computer
A. Multiple
B. Single
C. Double
D. Triple
Answer: B. Single

2. For a memory with a 20-bit address space, the addressability is
A. 16 bits
B. 8 bits
C. 2^20 bits
D. Cannot be determined
Answer: C. 2^20 bits

3. Because we wish to allow each ASCII code to occupy one location in memory, most memories are _____addressable.
A. BYTE
B. NIBBLE
C. WORD (16 bits)
D. DOUBLEWORD (32 bits)
Answer: A. BYTE

4. A structure that stores a number of bits taken "together as a unit" is a
A. gate
B. mux
C. decoder
D. register
Answer: D. register

5. We say that a set of gates is logically complete if we can build any circuit without using any other kind of gates. Which of the following sets are logically complete?
A. set of {AND, OR}
B. set of {EXOR, NOT}
C. set of {AND, OR, NOT}
D. None of the above

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Answer: C. set of {AND, OR, NOT}

6. If the number of address bits in a memory is reduced by 2 and the addressability is doubled, the size of the memory (i.e., the number of bits stored in the memory)
A. doubles
B. remains unchanged
C. halves
D. increases by 2^ (address bits)/addressability
Answer: C. halves

13. 'Burst refresh' in DRAM is also called
A.Concentrated refresh
B.Distributed refresh
C.Hidden refresh
D.None of the above
Answer: A. Concentrated refresh

14. An I/O processor controls the flow of information between
A.cache memory and I/O devices
B.main memory and I/O devices
C.two I/O devices
D.cache and main memory
Answer: B. main memory and I/O devices

15. The timing difference between a slow memory and fast processor can be
A.processor is capable of waiting
B.external buffer is used
C. either (a) or (b)
D.neither (a) nor (b)
Answer: C. either (a) or (b)

16. In 8086 the number of bytes which can be addressed directly is about
A. 1000
B. 10000
C. 100000
D. one million
Answer: D. one million

17. Which of the following is not a general purpose peripheral?
A.I/O port
B.Programmable interrupt controller
C.Programmable CRT controller
D.Programmable interval timer
Answer: C. Programmable CRT controller

18. Each instruction in assembly language program has the following fields:
Label field
Mnemonic Field
Operand Field
Comment field
The correct sequence of these fields is?
A. 1, 2, 3, 4
B. 1, 2, 4, 3
C. 2, 1, 3, 4
D. 2, 1, 4, 3
Answer: A. 1, 2, 3, 4

19. The operating modes of 8255 A are called
A. mode 0 and mode 1
B. mode 0, mode 1 and mode 2
C. mode 0 and mode 2
D. mode 0, mode 2 and mode 3
Answer: B. mode 0, mode 1 and mode 2

20. Internet is a worldwide network of computers where most of the information is freely available.
A.True
B. False
Answer: A.True

21. An e-mail message can be sent to many recipients.
A.True
B. False
Answer: A.True

22. Which memory has read operation, byte erase, byte write and chip erase?
A. RAM
B. UVEPROM
C.EEPROM
D. both (b) and (c)
Answer: C. EEPROM

23. The work of EU in 8086 is
A. Encoding
B. Decoding
C. Processing
D. Calculations
Answer: B. Decoding

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24. The 1MB Memory of 8086 can be divided into ---------- segments.

A. 1 Kbyte
B. 32 Kbyte
C. 64 Kbyte
D. 128 Kbyte
Answer: C. 64 Kbyte

25. The PUSH source copies a word from source to ----------
A. Stack
B. Memory
C. Register
D. Destination
Answer: A. Stack